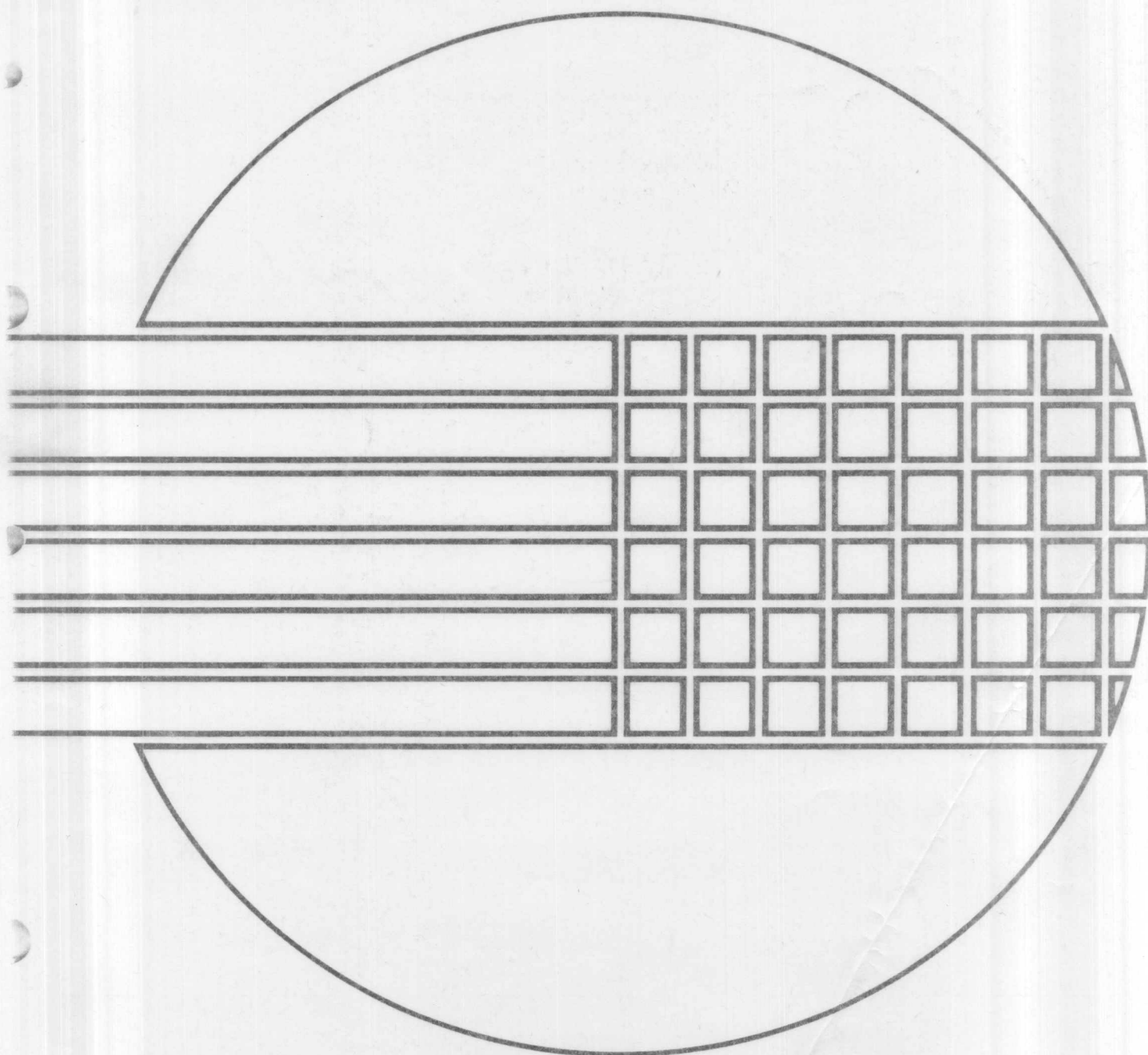


SIGNETICS

8-BIT μ -CHANNEL

MICROPROCESSOR

2650A



PRELIMINARY SPECIFICATION

DESCRIPTION

The 2650A and -1 are additional members of the Signetics family of 8 bit, NMOS microprocessors.

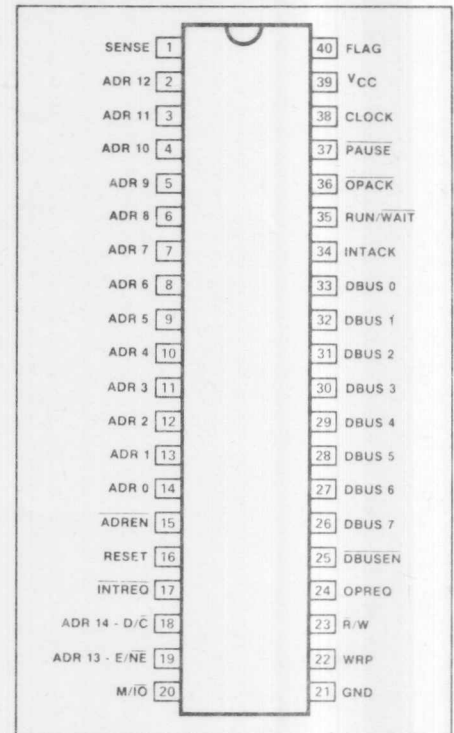
The 2650A is a functional equivalent of the 2650 with a new mask design which provides improved device operating margins.

The 2650A-1 is a high speed version of the 2650A.

FEATURES

- Static 8 bit parallel NMOS microprocessor
- Single power supply of +5 volts
- TTL level single phase clock
- Standard 40 pin dual in-line package
- TTL compatible inputs and outputs
- 75 variable length instructions of 1, 2 or 3 bytes
- 32K byte addressing range
- Coding efficiency with multiple addressing modes
- Synchronous or asynchronous memory and I/O interface
- Interfaces directly with industry standard memories
- Single bit serial I/O path
- Seven 8 bit addressable general purpose registers
- Vectored interrupt
- Subroutine return address stack
- 2.4 μ s machine cycle time (2650A)
- 1.5 μ s machine cycle time (2650A-1)

PIN CONFIGURATION



MICROPROCESSOR BLOCK DIAGRAM

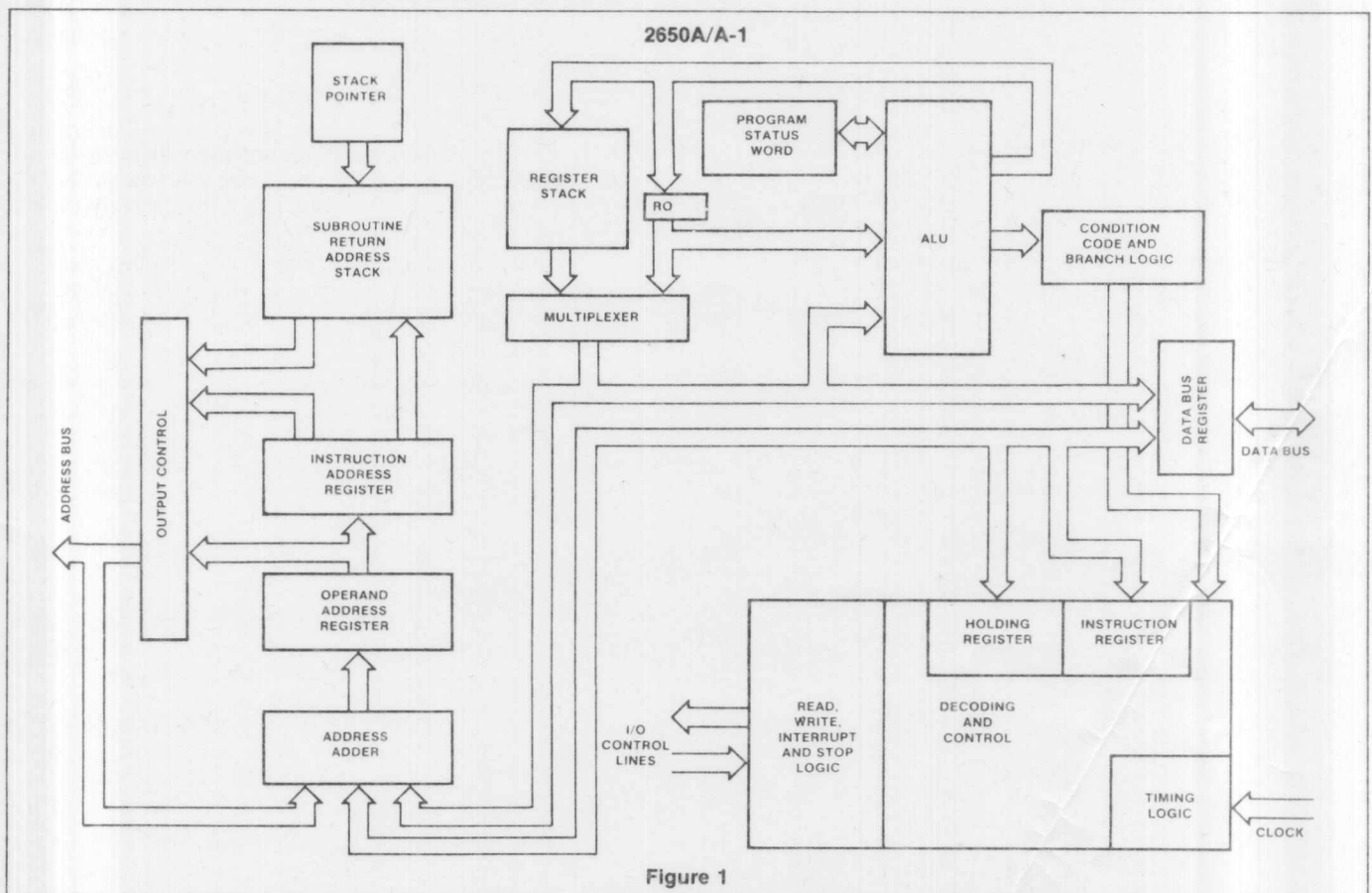


Figure 1

PRELIMINARY SPECIFICATION

PIN DESIGNATION

MNEMONIC	NUMBER	NAME	TYPE	FUNCTION
ADR0-ADR12	14-2	Address lines	O	Low order memory address lines for instruction or operand fetch. ADR0 is the least significant bit and ADR12 is the most significant bit. ADR0 through ADR7 are also used as the I/O device address for extended I/O instructions.
ADR13-E/ $\overline{\text{NE}}$	19	Address 13- Extended/Non Extended	O	Low order memory page address line during memory reference instructions. For I/O instructions this line discriminates between extended and non-extended I/O instructions.
ADR14-D/ $\overline{\text{C}}$	18	Address 14- Data/Control	O	High order memory page address line during memory reference instructions. It also serves as the I/O device address for non-extended I/O instructions.
$\overline{\text{ADREN}}$	15	Address enable	I	Active low input allowing tri-state control of the address bus ADR0-ADR12.
DBUS0-DBUS7	33-26	Data bus	I/O	These lines provide communication between the CPU, Memory, and I/O devices for instruction and data transfers.
$\overline{\text{DBUSEN}}$	25	Data bus enable	I	This active low input allows tri-state control of the data bus.
OPREQ	24	Operation request	O	Indicates to external devices that all address, data and control information is valid.
$\overline{\text{OPACK}}$	36	Operation acknowledge	I	Active low input indicating completion of an external operation. This allows asynchronous functioning of external devices.
M/ $\overline{\text{IO}}$	20	Memory/input-output	O	Indicates whether the current operation references memory or I/O.
$\overline{\text{R/W}}$	23	Read/Write	O	Indicates a read or a write operation.
WRP	22	Write pulse	O	This is a timing signal from the 2650 that provides a positive-going pulse during each requested write operation (memory or I/O) and a high level during read operations.
SENSE	1	Sense	I	The sense bit in the PSU reflects the logic state of the sense input to the processor at pin #1.
FLAG	40	Flag	O	The flag bit in the PSU is tied to a latch that drives the flag output at pin #40.
$\overline{\text{INTREQ}}$	17	Interrupt request	I	This active low input line indicates to the processor that an external device is requesting service. The processor will recognize this signal at the end of the current instruction if the interrupt inhibit status bit is zero.
INTACK	34	Interrupt acknowledge	O	This line indicates that the 2650 is ready to receive the interrupt vector (relative address byte) from the interrupting device.
$\overline{\text{PAUSE}}$	37	Pause	I	This active low input is used to suspend processor operation at the end of the current instruction.
RUN/ $\overline{\text{WAIT}}$	35	Run/Wait	O	This output is a processor status indicator. During normal operation this line is high. If the processor is halted either by executing a halt instruction or by a low input on the pause line, the run/wait line will go low.
RESET	16	Reset	I	Resets the instruction address register to zero and clears the interrupt inhibit bit.
CLOCK	38	Clock	I	A positive going pulse train that determines the instruction execution time.
V _{CC}	39	+5V	I	+5V power
GND	21	GND	I	Ground

PRELIMINARY SPECIFICATION

FUNCTIONAL DESCRIPTION

The 2650 series processors are general purpose, single chip, fixed instruction set, parallel 8-bit binary processors. A general purpose processor can perform any data manipulations through execution of a stored sequence of machine instructions. The processor has been designed to closely resemble conventional binary computers, but executes variable length instructions of one to three bytes in length.

The 2650 series contains a total of seven general purpose registers, each eight bits long. They may be used as source or destination for arithmetic operations, as index registers, and for I/O transfers.

The processor can address up to 32,768 bytes of memory in four pages of 8,192 bytes each. The processor instructions are one, two, or three bytes long, depending on the instruction. Variable length instructions tend to conserve memory space since a one-or-two byte instruction may often be used rather than a three byte instruction. The first byte of each instruction always specifies the operation to be performed and the addressing mode to be used. Most instructions use six of the first eight bits for this purpose, with the remaining two bits forming the register field. Some instructions use the full eight bits as an operation code.

The Data Bus and Address signals are tri-state to provide convenience in system design. Memory and I/O interface signals are asynchronous so that Direct Memory Access (DMA) and multiprocessor operations are easy to implement.

The block diagram for the 2650 series (Figure 1) shows the major internal components and the data paths that interconnect them. In order for the processor to execute an instruction, it performs the following general steps:

1. The Instruction Address Register provides an address for memory.
2. The first byte of an instruction is fetched from memory and stored in the Instruction Register.
3. The Instruction Register is decoded to determine the type of instruction and the addressing mode.
4. If an operand from memory is required, the operand address is resolved and loaded into the Operand Address Register.
5. The operand is fetched from memory and the operation is executed.
6. The first byte of the next instruction is fetched.

The Instruction Register (IR) holds the first byte of each instruction and directs the subsequent operations required to execute

each instruction. The IR contents are decoded and used in conjunction with the timing information to control the activation and sequencing of all the other elements on the chip. The Holding Register is used in some multiple-byte instructions to contain further instruction information and partial absolute addresses.

The Arithmetic Logic Unit (ALU) is used to perform all of the data manipulation operations, including Load, Store, Add, Subtract, And, Inclusive Or, Exclusive Or, Compare, Rotate, Increment and Decrement. It contains and controls the Carry bit, the Overflow bit, the Interdigit Carry and the Condition Code Register.

The Register Stack contains six registers that are organized into two banks of three registers each. The Register Select bit picks one of the two banks to be accessed by instructions. In order to accommodate the register-to register instructions, register zero (RO) is outside the array. Thus, register zero is always available along with one set of three registers.

The Address Adder is used to increment the instruction address and to calculate relative and indexed addresses.

The Instruction Address Register holds the address of the next instruction byte to be

accessed. The Operand Address Register stores operand addresses and sometimes contains intermediate results during effective address calculations.

The Return Address Stack (RAS) is a Last In, First Out (LIFO) storage which receives the return address whenever a Branch-to-Subroutine instruction is executed. When a Return instruction is executed, the RAS provides the last return address for the processor's IAR. The stack contains eight levels of storage so that subroutines may be nested up to eight levels deep. The Stack Pointer is a three bit wraparound counter that indicates the next available level in the stack. It always points to the current address.

PROGRAM STATUS WORD

The Program Status Word (PSW) is a major feature of the 2650 which greatly increases its flexibility and processing power. The PSW is a special purpose register within the processor that contains status and control bits.

It is divided into two bytes called the Program Status Upper (PSU) and Program Status Lower (PSL). The PSW bits may be tested, loaded, stored, preset, or cleared using the instructions which affect the PSW. The bits are utilized as shown in Table 1.

PSU0,1,2	SP	Pointer for the Return Address Stack.
PSU3,4		Not used. These bits are always zero.
PSU5	II	Used to inhibit recognition of additional Interrupts.
PSU6	F	Flag is a latch directly driving the flag output.
PSU7	S	Sense equals the state of the sense input.
PSL0	C	Carry stores any carry from the high-order bit of ALU.
PSL1	COM	Compare determines if a logical or arithmetic comparison is to be made.
PSL2	OVF	Overflow is set if a two's complement overflow occurs.
PSL3	WC	With Carry determines if the carry is used in arithmetic and rotate instructions.
PSL4	RS	Register Select identifies which bank of 3 GP registers is being used.
PSL5	IDC	Inter Digit Carry stores the bit-3 to-bit-4 carry in arithmetic operations.
PSL6,7	CC	Condition Code is affected by compare, test and arithmetic instructions.

PSU

7	6	5	4	3	2	1	0
S	F	II			SP2	SP1	SP0

S Sense
F Flag
II Interrupt Inhibit
SP2 Stack Pointer Two
SP1 Stack Pointer One
SP0 Stack Pointer Zero

PSL

7	6	5	4	3	2	1	0
CC1	CC0	IDC	RS	WC	OVF	COM	C

CC1 Condition Code One
CC0 Condition Code Zero
IDC Interdigit Carry
RS Register Bank Select
WC With/Without Carry
OVF Overflow
COM Logical/Arithmetic Compare
C Carry/Borrow

Table 1 PROGRAM STATUS WORD

PRELIMINARY SPECIFICATION

INPUT/OUTPUT INTERFACE

The 2650 series microprocessor has a set of versatile I/O instructions and can perform I/O operations in a variety of ways. One- and two-byte I/O instructions are provided, as well as a special single-bit I/O facility. The I/O modes provided by the 2650 are designated as Data, Control, and Extended I/O.

Data or Control I/O instructions, also called Non-Extended I/O instructions, are one byte long. Any general purpose register can be used as the source or destination. A special control line indicates if either a Data or Control instruction is being executed.

Extended I/O is a two-byte read or write instruction. Execution of an extended I/O instruction will cause a 8-bit address, taken from the second byte of the instruction, to be placed on the low order eight address lines. The data, which can originate or terminate with any general purpose register, is placed on the data bus. This type of I/O can be used to simultaneously select a device and send data to it.

Memory reference instructions that address data outside of physical memory may also

be used for I/O operations. When an instruction is executed, the address may be decoded by the I/O device rather than memory.

MEMORY INTERFACE

The memory interface consists of the address bus, the 8-bit data bus and several signals that operate in an interlocked or handshaking mode.

The Write Pulse signal is designed to be used as a memory strobe signal for any memory type. It has been particularly optimized to be used as the Chip Enable or Read/Write signal.

INTERRUPT HANDLING CAPABILITY

The 2650 series has a single level hardware vectored interrupt capability. When an interrupt occurs, the processor finishes the current instruction and sets the Interrupt Inhibit bit in the PSW. The processor then executes a Branch to Subroutine Relative to location Zero (ZBSR) instruction and sends out Interrupt Acknowledge and Operation Request signals. On receipt of the INTACK

signal the interrupting device inputs an 8-bit address, the interrupt vector, on the data bus. The relative and relative indirect addressing modes combined with this 8-bit address allow interrupt service routines to begin at any addressable memory location.

INSTRUCTION SET

It may be seen from examination of the 2650 instruction set that there are many powerful instructions which are all easily understood and are typical of larger computers. There are one-, two-, and three-byte instructions as a result of the multiplicity of addressing modes. See Table 2 for a complete listing and Figure 2 for instruction formats.

Automatic incrementing or decrementing of an index register is available in the arithmetic indexed instructions. All of the branch instructions except indexed branching can be conditional.

Register-to-register instructions are one byte; register-to-storage instructions are two or three bytes long. The two-byte register-to-memory instructions are either immediate or relative addressing types.

PRELIMINARY SPECIFICATION

	MNE- MONIG	DESCRIPTION OF OPERATION	OP CODE	PSW BITS								FOR-			NOTE			
			R or CC	AFFECTED								BYTES	CYCLES	MAT*				
			3	2	1	0	CC	IDC	C	OVF	SP	II	F					
LOAD/STORE	LOD	Z	03	02	01	—	•								1	2	Z	1
		I	07	06	05	04	•								2	2	I	1
		R	0B	0A	09	08	•								2	3	R	1,6
		A	0F	0E	0D	0C	•								3	4	A	6
	STR	Z	C3	C2	C1	—	•								1	2	Z	1
		R	CB	CA	C9	C8									2	3	R	6
A		CF	CE	CD	CC									3	4	A	6	
ARITHMETIC	ADD	Z	83	82	81	80	•	•	•	•					1	2	Z	1
		I	87	86	85	84	•	•	•	•					2	2	I	1
		R	8B	8A	89	88	•	•	•	•					2	3	R	1,6
		A	8F	8E	8D	8C	•	•	•	•					3	4	A	1,6
	SUB	Z	A3	A2	A1	A0	•	•	•	•					1	2	Z	1
		I	A7	A6	A5	A4	•	•	•	•					2	2	I	1
		R	AB	AA	A9	A8	•	•	•	•					2	3	R	1,6
		A	AF	AE	AD	AC	•	•	•	•					3	4	A	1,6
	DAR		97	96	95	94	•								1	3	Z	1,10
LOGICAL	AND	Z	43	42	41	—	•								1	2	Z	1
		I	47	46	45	44	•								2	2	I	1
		R	4B	4A	49	48	•								2	3	R	1,6
		A	4F	4E	4D	4C	•								3	4	A	1,6
	IOR	Z	63	62	61	60	•								1	2	Z	1
		I	67	66	65	64	•								2	2	I	1
		R	6B	6A	69	68	•								2	3	R	1,6
		A	6F	6E	6D	6C	•								3	4	A	1,6
	EOR	Z	23	22	21	20	•								1	2	Z	1
		I	27	26	25	24	•								2	2	I	1
		R	2B	2A	29	28	•								2	3	R	1,6
		A	2F	2E	2D	2C	•								3	4	A	1,6
ROTATE/COMPARE	COM	Z	E3	E2	E1	E0	•								1	2	Z	2
		I	E7	E6	E5	E4	•								2	2	I	3
		R	EB	EA	E9	E8	•								2	3	R	3,6
		A	EF	EE	ED	EC	•								3	4	A	3,6
	RRR		53	52	51	50	•	•	•	•					1	2	Z	1
	RRL		D3	D2	D1	D0	•	•	•	•					1	2	Z	1
BRANCH	BCT	R	1B	1A	19	18									2	3	R	7,8
		A	1F	1E	1D	1C									3	3	B	7,8
	BCF	R	—	9A	99	98									2	3	R	7
		A	—	9E	9D	9C									3	3	B	7
	BRN	R	5B	5A	59	58									2	3	R	7,8
		A	5F	5E	5D	5C									3	3	B	7,8
	BIR	R	DB	DA	D9	D8									2	3	R	7,8
		A	DF	DE	DD	DC									3	3	B	7,8

Table 4 INSTRUCTION SET SUMMARY

PRELIMINARY SPECIFICATION

	MNE- MONIC	DESCRIPTION OF OPERATION	OP CODE	PSW BITS								BYTES	CYCLES	FOR- MAT*	NOTE				
			R or CC	AFFECTED															
			3	2	1	0	CC	IDC	C	OVF	SP	II	F						
BRANCH (Cont'd)	BDR	R	Branch on decrementing register relative	FB	FA	F9	F8								2	3	R	7,8	
		A	Branch on decrementing register absolute	FF	FE	FD	FC								3	3	B	7,8	
	ZBRR	Zero branch relative, unconditional	9B	—	—	—									2	3	ER	6	
	BXA	Branch indexed absolute, unconditional	9F	—	—	—									3	3	EB	5,6	
SUBROUTINE BRANCH/RETURN	BST	R	Branch to subroutine on condition true, relative	3B	3A	39	38							•	2	3	R	7,8	
		A	Branch to subroutine on condition true, absolute	3F	3E	3D	3C								•	3	3	B	7,8
	BSF	R	Branch to subroutine on condition false, relative	—	BA	B9	B8								•	2	3	R	7
		A	Branch to subroutine on condition false, absolute	—	BE	BD	BC								•	3	3	B	7
	BSN	R	Branch to subroutine on non-zero register, relative	7B	7A	79	78								•	2	3	R	7,8
		A	Branch to subroutine on non-zero register, absolute	7F	7E	7D	7C								•	3	3	B	7,8
	ZBSR	Zero branch to subroutine relative, unconditional	BB	—	—	—										2	3	ER	6
	BSXA	Branch to subroutine, indexed, absolute unconditional	BF	—	—	—										3	3	EB	5,6
	RET	C	Return from subroutine, conditional	17	16	15	14								•	1	3	Z	8
		E	Return from subroutine and enable interrupt, conditional	37	36	35	34								•	•	1	3	Z
INPUT/OUTPUT	WRTD	Write data	F3	F2	F1	F0									1	2	Z		
	REDD	Read data	73	72	71	70	•								1	2	Z	1	
	WRTC	Write control	B3	B2	B1	B0									1	2	Z		
	REDC	Read control	33	32	31	30	•								1	2	Z	1	
	WRTE	Write extended	D7	D6	D5	D4									2	3	I		
	REDE	Read extended	57	56	55	54	•								2	3	I	1	
MISC.	HALT	Halt, enter wait state	—	—	—	40									1	1	E		
	NOP	No operation	—	—	—	C0									1	1	E		
	TMI	Test under mask immediate	F7	F6	F5	F4	•								2	3	I	4	
PROGRAM STATUS	LPS	U	Load program status, upper	92				•	•	•	•	•	•	•	1	2	E		
		L	Load program status, lower	93				•							1	2	E	9	
	SPS	U	Store program status, upper	12				•							1	2	E	1	
		L	Store program status, lower	13				•							1	2	E	1	
	CPS	U	Clear program status, upper, masked	74								•	•	•	2	3	EI		
		L	Clear program status, lower, masked	75				•	•	•	•				2	3	EI	9	
	PPS	U	Preset program status, upper, masked	76								•	•	•	2	3	EI		
		L	Preset program status, lower, masked	77				•	•	•	•				2	3	EI	9	
	TPS	U	Test program status, upper, masked	B4				•							2	3	EI	4	
L		Test program status, lower, masked	B5				•							2	3	EI	4		

*See Figure 2

Table 4 (Cont'd) INSTRUCTION SET SUMMARY

PRELIMINARY SPECIFICATION

NOTES

1. Condition code (CC1, CC0): 01 if positive, 00 if zero, 10 if negative.
2. Condition code (CC1, CC0): 01 if $R0 > r$, 00 if $R0 = r$, 10 if $R0 < r$.
3. Condition code (CC1, CC0): 01 if $r > V$, 00 if $r = V$, 10 if $r < V$.
4. Condition code (CC1, CC0): 00 if all selected bits are 1s, 10 if not all the selected bits are 1s.
5. Index register must be register 3 or 3'.
6. Requires two additional cycles if indirection is specified.
7. Requires two additional cycles if indirection is specified and branch is taken.
8. Specify CC = 11 for unconditional branch.
9. RS, WC and COM bits in PSW are also affected.
10. CC assumes number in register is a binary number.

ADDRESSING MODES

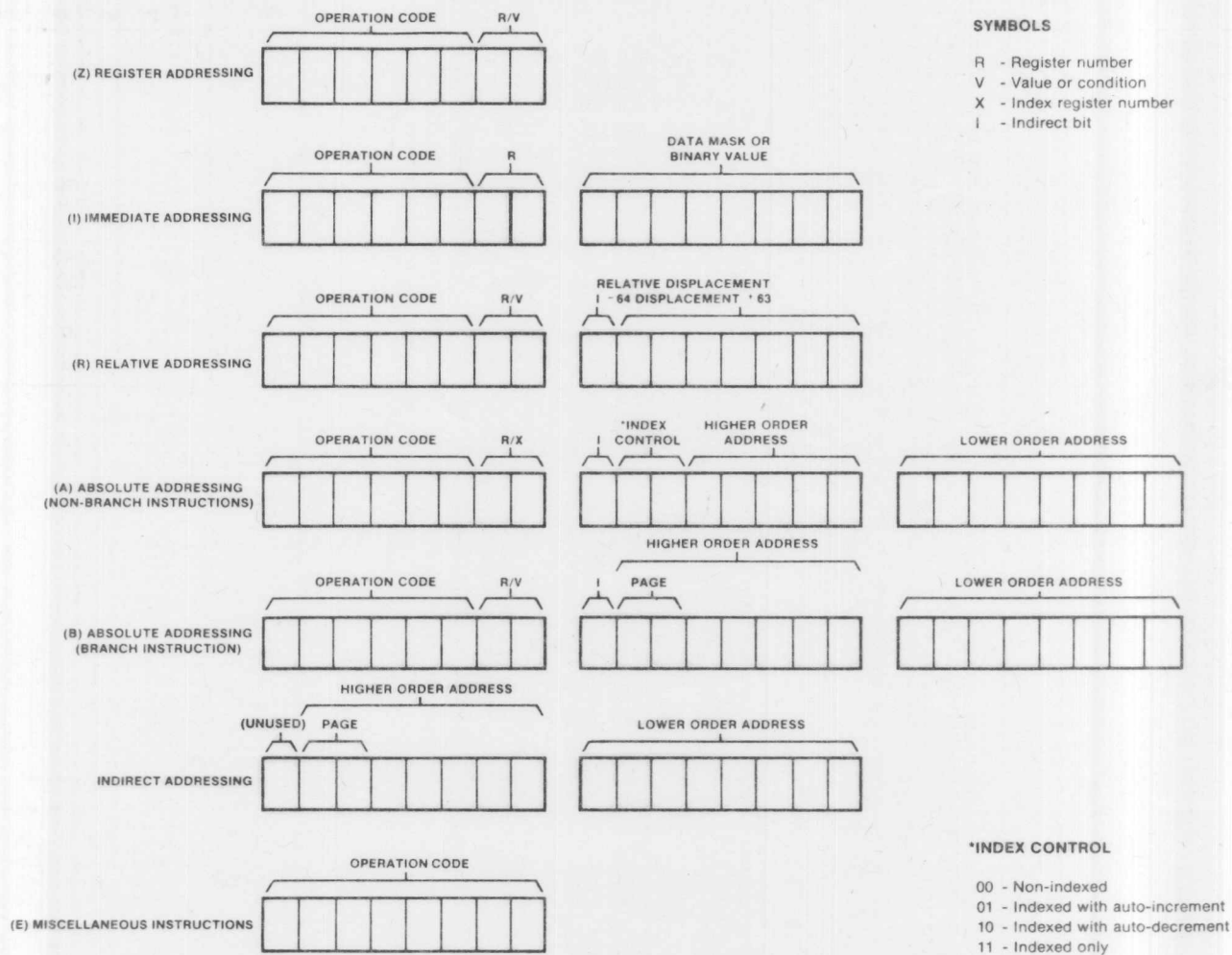


Figure 2

PRELIMINARY SPECIFICATION

ABSOLUTE MAXIMUM RATINGS¹

PARAMETER		RATING	UNIT
T _A	Operating temperature	0 to 70	°C
T _{STG}	Storage temperature	-65 to +150	°C
P _D	Package power dissipation ²	1.6	W
	All input, output, and supply voltages with respect to GND ³	-.5 to +6	V

DC ELECTRICAL CHARACTERISTICS T_A = 0°C to 70°C, V_{CC} = 5V ± 5%.

PARAMETER	TEST CONDITIONS	LIMITS			UNIT
		Min	Typ	Max	
I _{IL}	Current				μA
I _{LOH}	Input load			10	
I _{LOH}	Output high leakage			10	
I _{LOL}	Output low leakage			10	
	Voltage levels				V
V _{IH}	Input high	2.2		V _{CC}	
V _{IL}	Input low	-0.5		0.8	
V _{OH}	Output high	2.4			
V _{OL}	Output low	0.0		0.45	
I _{CC}	Power supply current			150	mA
	Capacitance				pf
C _{IN}	Input			10	
C _{OUT}	Output			10	

NOTES

- Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operation sections of this specification is not implied.
- For operating at elevated temperatures the device must be derated based on +150°C maximum junction temperature and thermal resistance of 50°C/W junction to ambient (40 pin IW package).
- This product includes circuitry specifically designed for the protection of its internal devices from the damaging effects of excessive static charge. However, it is suggested that conventional precautions be taken to avoid applying any voltages larger than the rated maxima.
- Parameters valid over operating temperature range unless otherwise specified.
- All voltage measurements are referenced to ground.
- Preliminary specification
- Manufacturer reserves the right to make design and process changes and improvements.

PRELIMINARY SPECIFICATION

AC ELECTRICAL CHARACTERISTICS $T_A = 0^\circ\text{C}$ to $+70^\circ\text{C}$, $V_{CC} = +5V \pm 5\%$.

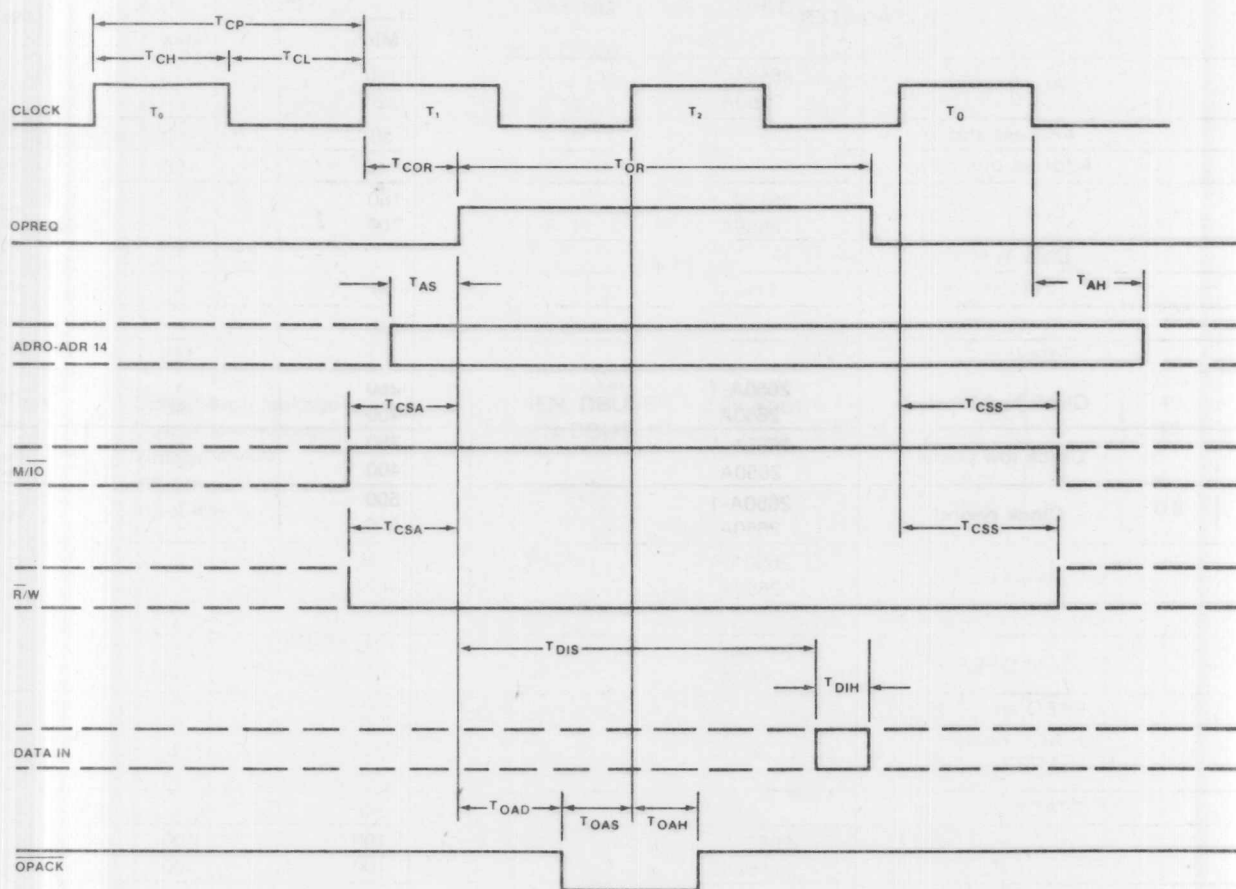
PARAMETER			LIMITS		UNIT
			Min	Max	
T_{AH}	Address hold	2650A-1 2650A	180 220		ns
T_{AS}	Address stable		50	-	ns
T_{ABD}	Address bus delay		-	180	ns
T_{DH}	Data out hold	2650A-1 2650A	160 200		ns
T_{DIS}	Data in stable		-	$2T_{CH} + T_{CL} - 200$	ns
T_{DS}	Data stable		50	-	ns
T_{DIH}	Data in hold		50	-	ns
T_{DBD}	Data bus delay		-	150	ns
T_{CH}	Clock high phase	2650A-1 2650A	250 400	- -	ns
T_{CL}	Clock low phase	2650A-1 2650A	250 400	- -	ns
T_{CP}	Clock period	2650A-1 2650A	500 800	- -	ns
$T_{PC(5)}$	Processor cycle time	2650A-1 2650A	1500 2400	- -	ns
T_{OR}	OPREQ pulse width ⁷		$2 T_{CH} + T_{CL}$	$2 T_{CH} + T_{CL} + 100$	ns
T_{COR}	Clock to OPREQ time	2650A-1 2650A	100 150	200 300	ns
T_{OSD}	OPREQ signal delay		-	230	ns
T_{OAD}	OPACK delay time		0	-	ns
T_{OAS}	OPACK setup time		50	-	ns
T_{OAH}	OPACK hold time		50	-	ns
T_{CSS}	Control signal stable	2650A-1 2650A	100 100	400 500	ns
T_{CSA}	Control signal available		200	-	ns
T_{WPD}	Write pulse delay	2650A-1 2650A	100 100	200 300	ns
T_{WPO}	Write pulse from OPREQ		$T_{CH} - 100$	$T_{CH} + 150$	ns
T_{WPW}	Write pulse width ⁷		$T_{CH} - 75$	T_{CH}	ns
T_{IRS}	INTREQ set up time		-	150	ns
T_{IRH}	INTREQ hold time		0	-	ns
T_{CSD}	Control signal delay		-	180	ns

NOTES

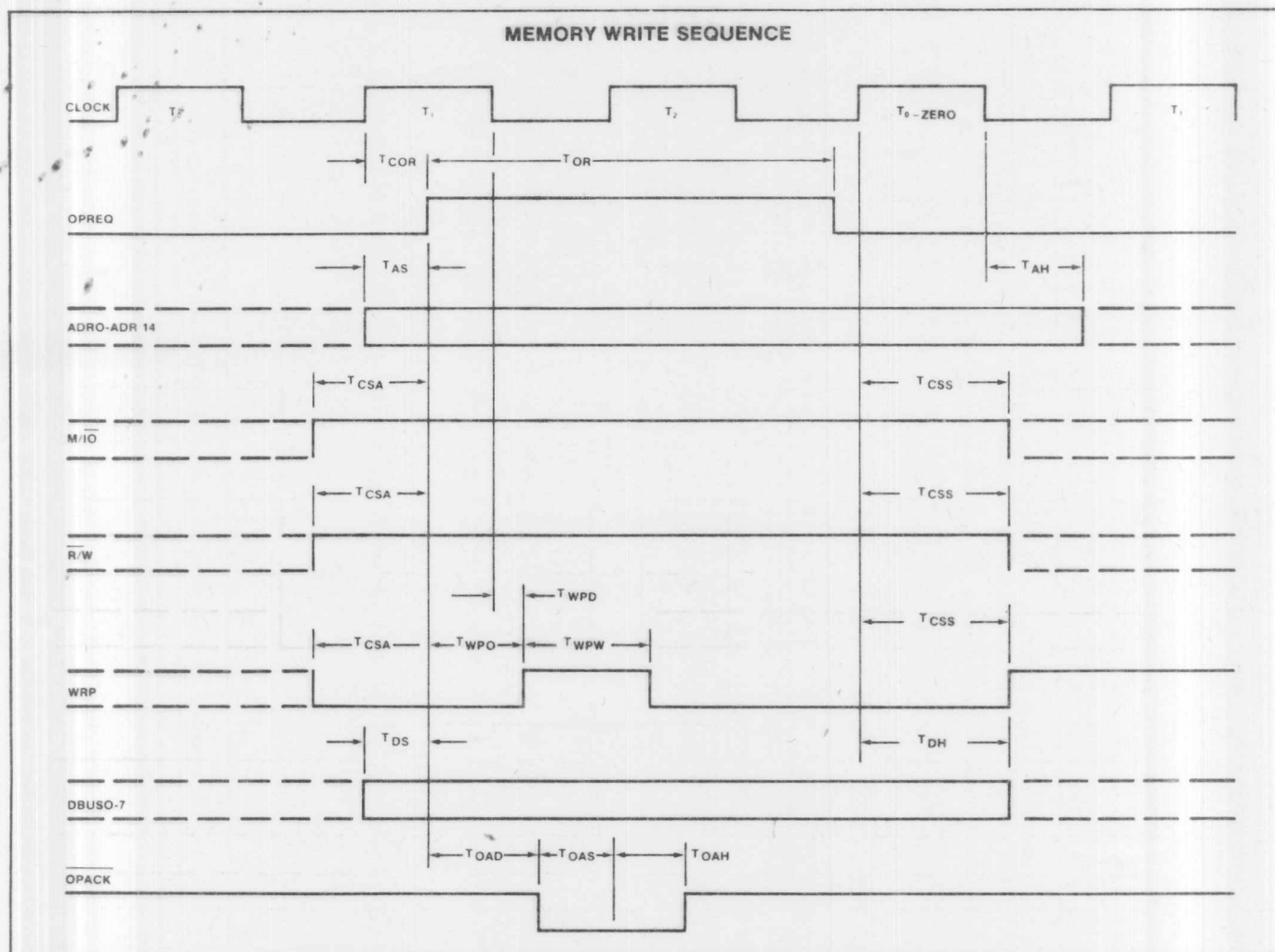
1. Input levels swing between 0.80 and 2.2 volts.
2. Input signal transition times are 20ns.
3. Timing reference level is 1.5 volts.
4. Output load is $-100\ \mu\text{A}$ at 100pf and 1 TTL load.
5. Processor cycle time consists of three clock periods.
6. Output buffer rise time is 150ns maximum.
7. These values assume that OPACK is returned in time to not cause the processor to idle. Otherwise, the specified maximum will increase by an internal number of clock cycles.

PRELIMINARY SPECIFICATION

MEMORY READ SEQUENCE



PRELIMINARY SPECIFICATION



PRELIMINARY SPECIFICATION

